

526, 197  
10/526197

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property  
Organization  
International Bureau



(43) International Publication Date  
18 March 2004 (18.03.2004)

PCT

(10) International Publication Number  
**WO 2004/023656 A1**

(51) International Patent Classification<sup>7</sup>: H03L 7/093, 7/18

(21) International Application Number:  
PCT/IB2003/003771

(22) International Filing Date: 22 August 2003 (22.08.2003)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:  
0220616.7 5 September 2002 (05.09.2002) GB

(71) Applicant (for all designated States except US): KONINKLIJKE PHILIPS ELECTRONICS N.V. [NL/NL]; Groenewoudseweg 1, NL-5621 BA Eindhoven (NL).

G. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB). MARSHALL, Paul, R. [GB/GB]; c/o Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(74) Agent: WHITE, Andrew; Philips Intellectual Property & Standards, Cross Oak Lane, Redhill, Surrey RH1 5HA (GB).

(81) Designated States (national): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NO, NZ, OM, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

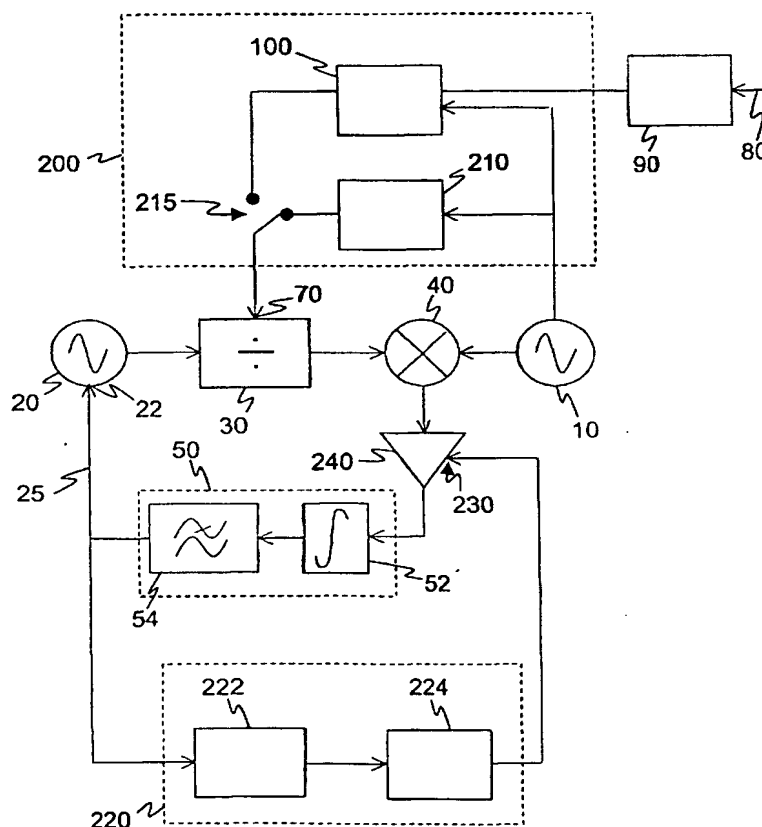
(72) Inventors; and

(75) Inventors/Applicants (for US only): SPENCER, Adrian,

(84) Designated States (regional): ARIPO patent (GH, GM, KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZM, ZW),

[Continued on next page]

(54) Title: IMPROVEMENTS RELATING TO PHASE-LOCK LOOPS



(57) Abstract: A phase lock loop comprises a variable frequency oscillator (20), a divider (30), a phase comparator (40), a gain control stage (240), and a loop filter (50). The frequency response of the loop is measured by superimposing a modulation at a number of different rates on the error signal generated by the phase comparator, and by measuring for each modulation rate the peak-to-peak variation of the loop control signal controlling the oscillator frequency. If, due to errors in component values, the frequency response deviates from its desired value, the loop gain is adjusted to bring the frequency response close to its desired value.

WO 2004/023656 A1